UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,258	12/06/2001	Nobuyuki Ohminami	829-593	4463

7590 09/07/2004

NIXON & VANDERHYE P.C.
8th Floor
1100 North Glebe Road
Arlington, VA 22201-4714

EXAMINER	
HAMDAN, WASSEEM H	

ART UNIT	PAPER NUMBER
2854	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,258	OHMINAMI, NOBUYUKI	
	Examiner	Art Unit	
	Wasseem H Hamdan	2854	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 10* is/are allowed.

6)☒ Claim(s) *1-3 and 5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lab1 – Capacitance Measurement (Physics 3 Spring 1989) in view of Japanese Patent Laid-Open No. 06-112289 (inventor: Kono Motohiro et al.).

Regarding claims 1, 7 and 8, "Physics 3, Lab 1" discloses an insulator capacitance analyzer for analyzing C-V characteristics [Figure 3] of a first structure having unknown capacitance [C_2], comprising:

a capacitance structure having known capacitance [C_1] and configured so as to be serially connected [Figure 3] to the first structure [C_2]; and
a measuring section [page 4/7, third section], for measuring synthesis capacitance [page 4/7, third section].

Regarding claims 1, 2, 7, 8 and 9, "Physics 3, Lab 1" discloses the essential elements of the claimed invention except for MIS structure. Kono et al. discloses MIS structure [page 15 (Drawing 2; page 4 [0013]]. It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to modify the teachings of "Physics 3, Lab 1" by

including MIS structure, since it would be beneficial for the purpose of measuring electric characteristics of a semiconductor wafer, such as C-V curve.

Regarding claims 2 and 9, "Physics 3, Lab 1" discloses at least one of a second MIS, a dielectric, and a capacitor [page 2/7, equations 1 and 2, based on the basic theory of the capacitance C-V measurement, one ordinary skill in the art at the time of the invention would able to add as many capacitors as the design is needed].

Regarding claim 7, "Physics 3, Lab 1" discloses the essential elements of the claimed invention except for calculating capacitance of the unknown capacitance based on the synthesis capacitance. Kono et al. discloses calculating capacitance of the unknown capacitance based on the synthesis capacitance [section 0016]. It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to modify the teachings of "Physics 3, Lab 1" by including calculating capacitance of the unknown capacitance based on the synthesis capacitance, since it would be beneficial for the purpose of measuring electric characteristics of a semiconductor wafer, such as C-V curve.

Regarding claim 3, "Physics 3, Lab 1" discloses wherein the capacitance structure is configured so as to be removable from the insulator capacitance analyzer [Figure 3].

2. Claims 5 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Lab1 – Capacitance Measurement (Physics 3 Spring 1989) in view of Japanese Patent Laid-Open No.

06-112289 (inventor: Kono Motohiro et al.) as applied to claims 1-3 and 7-9 above, and further in view of in view of Japanese Patent Laid-Open No. 1 1-150246 (OKI Electric IND LTD).

Regarding claim 5, "Physics 3, Lab 1" and Kono together disclose the essential elements of the claimed invention. However, Physics 3, Lab 1 does not explicitly wherein the equivalent silicon oxide thickness of the capacitance of the capacitance structure is 3 nm or more. Japanese Patent Laid-Open No. 11-150246 discloses wherein the equivalent silicon oxide thickness of the capacitance of the capacitance structure is 3 nm or more [English abstract]. It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to further modify the teachings of "Physics 3, Lab 1" by further including the equivalent silicon oxide thickness of the capacitance of the capacitance structure is 3 nm or more. The skilled artisan would have been motivated to modify "Physics 3, Lab 1" as above for because the appropriate thickness of silicon oxide film prevents leakage current [Japanese Patent Laid-Open No. 11150246: advantage].

Regarding claim 6, "Physics 3, Lab 1" and Kono together disclose the essential elements of the claimed invention. However, "Physics 3, Lab 1" does not explicitly the capacitance structure is configured so as to prevent direct tunnel leakage current from flowing through the capacitance Structure. Japanese Patent Laid-Open No. 1 1-150246 discloses wherein the capacitance structure is configured so as to prevent direct tunnel leakage current from flowing through the capacitance structure [Japanese Patent Laid-Open No. 11-150246: advantage]. It would have been obvious to a person having ordinary skill in the art at the time of the invention was made to modify the teachings of "Physics 3, Lab 1" by including wherein the capacitance

structure is configured so as to prevent direct tunnel leakage current from flowing through the capacitance structure. The skilled artisan would have been motivated to modify "Physics 3, Lab 1" as above for because the appropriate thickness of silicon oxide film prevents leakage current [Japanese Patent Laid-Open No. 11-150246: advantage].

Allowable Subject Matter

3. Claims 4 and 10 are allowed.

Response to Arguments

4. In response to applicant's argument on pages 3 and 4, that "there is absolutely no showing of record indicating that the newly cited document entitled "Physics 3 Spring 1989 - Lab 1 - Capacitance Measurements" (Lab1) is "prior art" to the instant invention. Lab1 appears to have been found during a recent internet search by the USPTO - clearly performed well after the instant application was filed. importantly, there is no evidence indicating that Lab1 was "published" prior to December 12, 2000. Instead, Lab1 appears to have come from a student's lab notebook indicative of lab experiments performed at Dartmouth College - possibly in 1989. Such a lab notebook is not "prior art" to the instant application unless it was "published" or was a "printed publication" prior to December 12, 2000. Clearly, lab notebooks typically are not "printed publications" or "published" in the United States." The examiner respectfully disagrees, because the "Physics 3 Spring 1989 - Lab 1 - Capacitance Measurements" is publication from a US university for students to work a lab session, it is not a student notebook, therefore it is a publication and it is considered to be a prior art. Therefore the rejection is proper.

Applicant's arguments on page 4, that " Kono is insufficient for the reasons set forth in the Appeal Brief dated November 10, 2003, the disclosure of which is hereby incorporated herein by reference. Moreover, one of ordinary skill in the art if measuring the MAIS structure of Kono would never have used a contact-type device because Kono teaches directly to the contrary. In particular, Kono teaches that one of ordinary skill in the art measuring a MAIS structure as in Kono would not use a contact-type device, thereby teaching directly away from the invention of claim 1. Yet another reason why the alleged combination fails is that Kono's VoMAls is not a capacitance structure with known capacitance. Kono discloses a single MAIS structure (the MIS is an ideal or imagined structure calculated from measurements performed on the MAIS). ..." The examiner respectfully disagrees, because as set forth in the office action that Kono is not being modifies, on the contrary, "Physics 3, Lab 1" is being modified. Therefore the argument is moot. Also the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). Therefore the rejection is proper.

Applicant's arguments on pages 5 and 6, that "the MIS structure of Kono is hypothetical and calculated from the measurements performed on the MAIS structure, in other words, Kono discloses using a Metal/Air/Insulator/semiconductor (MAIS) structure - but not directly

analyzing any MIS structure. In this respect, Kono determines measurements using a MAIS, and then uses these measurements to approximate what characteristics would be of a hypothetical MIS. This is because, as explained above, Kono's device is not capable of analyzing a MIS structure. Accordingly, it can be seen that, contrary to claim 1, the device of Kono ..." The examiner respectfully disagrees, because with the broadest reasonable interpretation of the claimed limitation, the Lab1 – Capacitance Measurement (Physics 3 Spring 1989) in view of Japanese Patent Laid-Open No. 06-112289 (inventor: Kono Motohiro et al.) do read on the claim language.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wasseem H Hamdan whose telephone number is (571) 272-2166. The examiner can normally be reached on M-F (first Friday off) 6:30 AM- 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew H Hirshfeld can be reached on (571) 272-2168. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wasseem H. Hamdan

August 31, 2004

ANDREW H. HIRSHFELD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Physics 3 Spring 1989
Lab 1 - Capacitance Measurements

Theory

In this laboratory we will use some simple equipment - a variable 0-5 V power supply and a 5 VDC electrometer (approximately an ideal voltmeter) - to: (1) experimentally confirm the expressions for equivalent capacitances for series, parallel and compound circuits and (2) to measure the capacitance of an unknown capacitor by two methods, charge sharing and voltage ratio measurements.

Equivalent Capacitance

Consider the circuits shown in figure 1. For each of these circuits, it is a straight forward

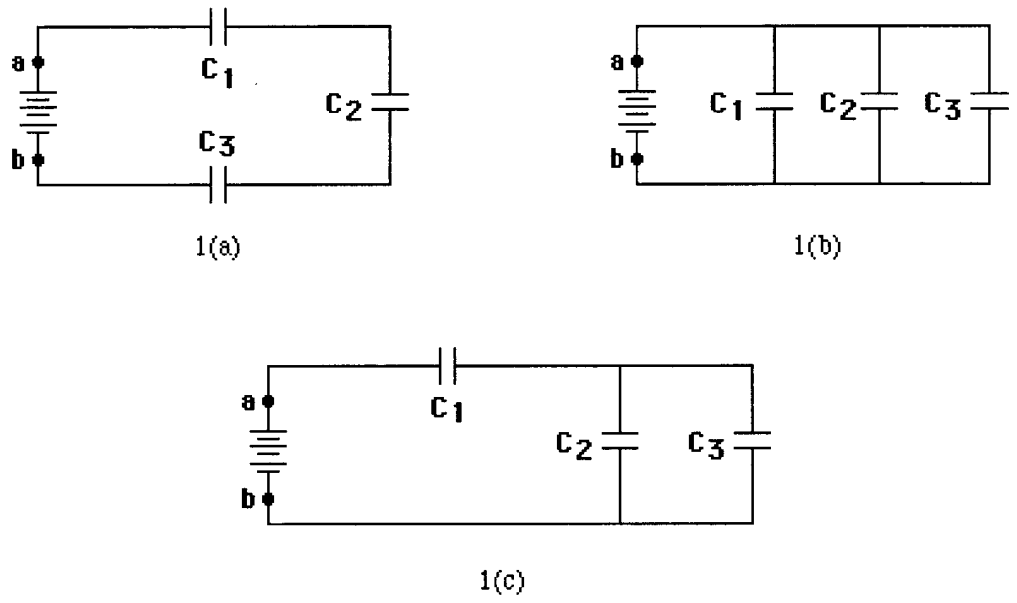

Figure 1

matter to calculate the total capacitance of the circuit (the capacitance between the points a and b). For simple series capacitive circuits such as the one depicted in Figure 1a, the total capacitance is given by

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \ldots + \frac{1}{C_N} \quad ; \quad (1)$$

and for simple parallel capacitive circuits such as depicted in Figure 1b, the total capacitance is given by

$$C_T = C_1 + C_2 + C_3 + \ldots + C_N \quad . \quad (2)$$

The derivations of these two expressions will be left to the reader.

The third circuit (Figure 1c) cannot be classified as either a simple series or simple parallel capacitive circuit. Circuits of this type can often, however, still be analyzed with the use of the equations (1) and (2) by using the concept of equivalent circuits. This concept states that any group of capacitors in a simple series or simple parallel arrangements can be replaced by a single capacitor which would leave unaltered the potential difference between the terminals of the group and the current in the rest of the circuit. The value of the single capacitor can be determined using equations (1) and (2). The circuit with the single capacitor is externally equivalent in every respect to the original circuit. Circuit analysis then becomes a matter of reducing each series and parallel capacitive subgroup in a combination circuit to its equivalent capacitance until what is left is a simple series or simple parallel circuit. Using this technique the total capacitance for the circuit in figure 1c would be given by

$$\frac{1}{C_2} = \frac{1}{C_1} + \frac{1}{C_2 + C_3} \quad .$$

Charge Sharing and Voltage Ratio Capacitance Measurements

Charge Sharing. Consider the circuit shown in Figure 2. It can be shown that if a capacitor C_1 is initially charged to a potential difference V_o by connecting it across a power supply and is then

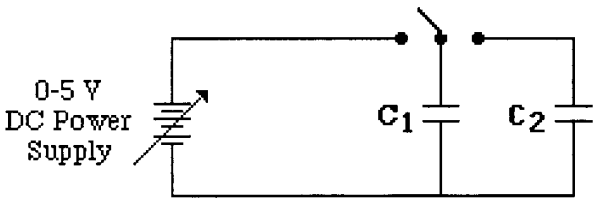

Figure 2

disconnected and(figure 2)reconnected across an uncharged capacitor C_2, the final potential difference across the combination V is given by

$$V = V_o \frac{C_1}{C_1 + C_2} \quad . \quad (3)$$

If we know C_1 and have a voltmeter to measure V_o and V, then this relationship can be used to measure the capacitance of one capacitor C_2, say, in terms of the capacitance of another known capacitance C_1. From equation (3), we see that the final potential across C_1 is always smaller than the initial potential across C_1. This is due to the fact that the charge placed on C_1 by the power supply is shared with C_2 when they are connected together. Hence, this technique for measuring the unknown capacitance of C_2 is called the charge sharing method.

Voltage Ratio. Consider the circuit shown in figure 3. It can be shown that when two initially uncharged capacitors C_1 and C_2 are connected to a voltage source in series as shown, the voltages

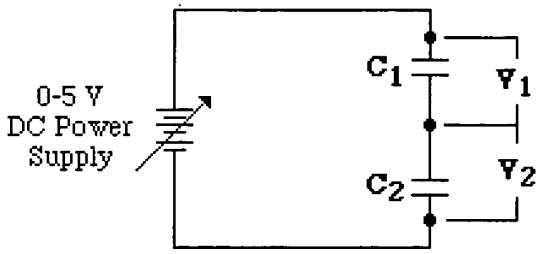

Figure 3

across the individual capacitors are related to the individual capacitances by the expression.

$$\frac{V_1}{V_2} = \frac{C_2}{C_1} \qquad . \quad (4)$$

If we know C_1 and have a voltmeter to measure V_1 and V_2, this relationship can also be used to determine an unknown capacitance C_2 in terms of the other capacitance C_1 and the voltage ratio V_1/V_2. For obvious reasons, this technique for measuring the unknown capacitance C_2 is called the voltage ratio method.

References

The sections in Bueche which are pertinent to this laboratory are chapter 20 sections 20.5 - 20.6 and 20.13. They should be read before coming to lab.

Experimental Purpose

The specific experimental purposes of this laboratory are the following:

1. to experimentally confirm the equivalent capacitance relationship for series

$$\left(\frac{1}{C_T} = \sum_i \frac{1}{C_i}\right)$$

and parallel

$$\left(C_T = \sum_i C_i\right)$$

capacitance circuits;

2. to experimentally confirm the theoretically predicted equivalent capacitance for two combination circuit;

3. to experimentally confirm the capacitance relationships in a homework problem given in the lab writeup;

4. to experimentally measure the capacitance of an unknown capacitor using two methods - charge sharing and volt age ratio; and

5. to experimentally measure the capacitance of an unknown with a capacitance << than the standard using the repeated charge sharing method.

Procedure

Before beginning please note the following:

a. The electrometer is a very sensitive instrument. To prevent damage to its components, do not turn it on without a capacitor connected across its terminals. The power switch is a toggle switch located to the right of the voltage scale. The electrometer is on when the switch is in the up position.

b. Before carrying out any measurements be sure to discharge all capacitors. This can be done by touching the metal wires on the capacitors to some well grounded metal surface such as a metal stool, a water pipe or the casing of the power supply. You should check to see that the capacitor is totally discharged by connecting it to the electrometer and observing whether or not the electrometer reads zero.

c. Finally, the wires on the capacitors are fragile. Please bend them as little as possible.

1. Using various series and parallel combinations of the marked (±10% precision) capacitors, verify equations (1) and (2) for equivalent capacitance of series and parallel connected capacitors by charge sharing experiments with your standard capacitor. This can be done by following these steps:

a. discharge all capacitors;

b. connect your standard capacitor to the terminals of the electrometer by inserting its wires through the holes in the terminal posts and tightening the red and black terminal caps;

c. using the red bread board and white connecting strips, construct the series or parallel circuit you wish to use;

d. connect the power supply to the terminals of the electrometer, (observing the correct polarity) and place a voltage of 5 V across the known capacitor;

e. disconnect the power supply from the electrometer and connect the terminals of the series or

parallel circuit to the terminals of the electrometer (your series or parallel circuit becomes C_2 in equation (3));

f. record the final voltage and compute the total capacitance of the circuit using equation (3).

Compare your experimentally measured values of C_T with the theoretical values of C_T calculated using the capacitances marked on the individual capacitor cases and equations (1) and (2). Note that the values marked on the standard capacitor are in pico-facads while the values given on all other capacitors are in micro-farads (1 pico-farad = 10-6 micro-farad).

2. Measure the equivalent capacitance of the two combinations of capacitors shown below using the same methods as procedure 1 and compare your results with the theoretically predicted values based upon the given individual capacitances.

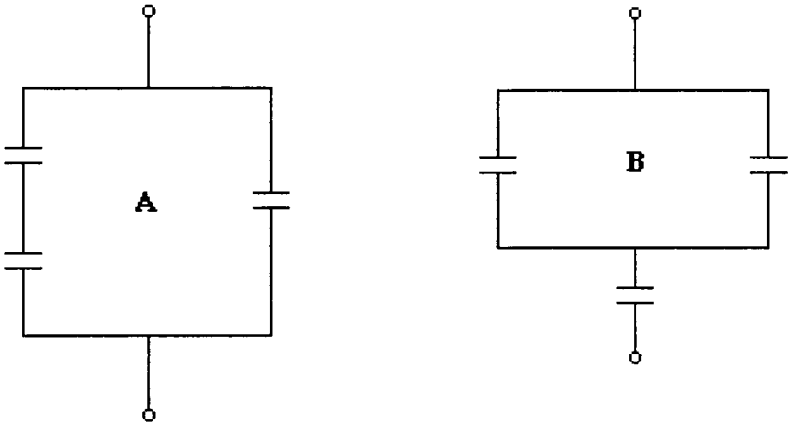

Figure 4

3. Answer the following questions (taken from Halliday and Resnick third edition p. 670) and experimentally verify all of the potential relationships. "A potential difference of 3.0 V is applied to a .01 μf capacitor and an .02 μf capacitor connected series.

   a. What are the charge and potential difference for each capacitor?

   b. The charged capacitors are reconnected with their positive plates together and their negative plates together, no external voltage being applied. What are the charge and potential difference for each?

   c. The charged capacitors in (a) are reconnected with plates of opposite sign together. What are the charge and the potential difference for each?

   With these and all future measurements it will be left to the reader to determine the best way to make the necessary measurements.

4. Measure the capacitance of the unknown black capacitor using both methods (charge sharing

and voltage ratio) described in the introduction. Use the standard calibrated capacitor provided as your known capacitance. Interchange C_1 and C_2 and repeat the measurements. Determine a best value for your unknown capacitance and estimate the uncertainty in your result. Be sure to record the number of your unknown capacitor.

5. If the capacitance of the unknown capacitor is << than the capacitance of the known capacitor, one charge sharing will not yield an accurate value for the unknown capacitance. (Why?) It can be shown, however, that if the charge sharing is repeated n times (the unknown being discharged before each charge sharing), then the unknown capacitance is given by the expression

$$C_2 = C_1\left[\left(\frac{V_o}{V_f}\right)^{1/n} - 1\right] \qquad (5)$$

where C_1 and C_2 are the known and unknown capacitances respectively, V_o is the initial potential difference across the known capacitor and V_f is the potential difference across the known capacitor after n charge sharings. Use this repeated charge sharing method to mea sure the capacitance of the unknown marked "US". Again be sure to record the number of your unknown capacitor. Use a value 5 V for V_o and use a value of n large enough to make $V_f \leq 2.5$ V.

When you are done, disconnect all capacitors, unplug the power supply and turn off the electrometer.

Lab Report

Your lab notebook will be your lab report. Be sure to include the following in your notebook:

1. all raw data;
2. derivations of equations (1) - (5) ;
3. samples of all theoretical calculations done;
4. a theoretical solution to the problem given in procedure 3;
5. calculations of the percent deviation between all theoretical predictions and the
6. a brief discussion of the sources of error in the measurement;
7. a discussion of how well (in terms of your answers to numbers 5 and 6 above) you feel your your experimental measurements agree with theory.